ME310M1

Interfaces User Guide

1VV0301970 Rev.0
2024-04-04
Released
Confidential

Technical Documentation

Contents

1 Applicability Table 3
2 Introduction 4
2.1 Scope 4
2.2 Audience 4
2.3 Contact Information, Support 4
2.4 Conventions 4
2.5 Terms and conditions 5
2.6 Disclaimer 5
3 General Product Description 6
3.1 Overview 6
4 ME310M1 INTERFACE TLB for EVB 2.0 7
4.1 Description 7
4.2 Physical Dimensions 7
4.3 Interface Details 8
Connectors Position 8
Jumpers Setting 10
5 PL101, PL102, PL103 – EVB 2.0 Connection 11
6 Antenna Connectors 13
6.1 SO304 – MAIN Antenna Connector 13
6.2 SO303 – GNSS Antenna Connector 13
6.3 WAKEUP push button 13
7 SIM selector Connector 14
7.1 PL201 14
8 Expansion Connectors 15
8.1 PL401 15
9 ANNEX 1 ME310M1 Interface TLB Schematic 17
10 ANNEX 2 ME310M1 Interface TLB Components Layout 23
11 Acronyms and Abbreviations 28
12 Related Documents 29
13 Document History 30

1 Applicability Table

Table 1: Applicability Table

Products
ME310M1-W2 Interface TLB
ME310M1-W1 Interface TLB

2 Introduction

2.1 Scope

The aim of this document is the handling description of the Interfaces for the ME310M1 products based on xE310 form factor.

2.2 Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit module.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: https://www.telit.com/contact-us/

Product information and technical documents are accessible 24/7 on our website: https://www.telit.com

2.4 Conventions

Note:	Provide advice and suggestions that may be useful when integrating the module.
Danger:	This information MUST be followed, or catastrophic equipment failure or personal injury may occur.
Warning:	Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and conditions

Refer to https://www.telit.com/hardware-terms-conditions/.

2.6 Disclaimer

THE MATERIAL IN THIS DOCUMENT IS FOR INFORMATIONAL PURPOSES ONLY. TELIT CINTERION RESERVES THE RIGHT TO MAKE CHANGES TO THE PRODUCTS DESCRIBED HEREIN. THE SPECIFICATIONS IN THIS DOCUMENT ARE SUBJECT TO CHANGE AT THE DISCRETION OF TELIT CINTERION WITHOUT PRIOR NOTICE. THIS DOCUMENT IS PROVIDED ON “AS IS” BASIS ONLY AND MAY CONTAIN DEFICIENCIES OR INADEQUACIES. TELIT CINTERION DOES NOT ASSUME ANY LIABILITY FOR INFORMATION PROVIDED IN THE DOCUMENT OR ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT DESCRIBED HEREIN.

TELIT CINTERION GRANTS A NON-EXCLUSIVE RIGHT TO USE THE DOCUMENT. THE RECIPIENT SHALL NOT COPY, MODIFY, DISCLOSE, OR REPRODUCE THE DOCUMENT EXCEPT AS SPECIFICALLY AUTHORIZED BY TELIT CINTERION.

TELIT CINTERION AND THE TELIT CINTERION LOGO, ARE TRADEMARKS OF TELIT CINTERION AND ARE REGISTERED IN CERTAIN COUNTRIES. ALL OTHER REGISTERED TRADEMARKS OR TRADEMARKS MENTIONED IN THIS DOCUMENT ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS AND ARE EXPRESSLY RESERVED BY TELIT CINTERION (AND ITS LICENSORS).

3 General Product Description

3.1 Overview

The Telit EVB 2.0 provides a robust, future-proof and flexible environment to streamline all application development based on Telit GSM/GPRS, UMTS/HSPA, CDMA 1x/EV-DO, and LTE module families, significantly reducing time-to-market.

The EVB 2.0 includes a motherboard where to connect the Interface board of a Telit module.

This concept allows the EVB 2.0 to be used across various form factors and product generations, both present and future.

The motherboard includes the basic interfaces such as power input, SIM card holder, audio monitor outputs, RS-232, and USB; as well as a Reset button and power switch.

The circuit parts implemented in the EVB 2.0 motherboard can be used as examples, but in a typical application they can often be simpler.

Adapter boards are available for all the different module families.

The part of the basic interfaces is served by the motherboard, whereas specific interfaces according to the type of the module (antenna, general purpose inputs/outputs GPIO, ADC/DAC, UART) are available on the adapter board to connect it to the user applications, extension boards, measurements equipment or other tools.

4 ME310M1 INTERFACE TLB for EVB 2.0

4.1 Description

This board allows easily interfacing the ME310M1 modules with the Telit EVB 2.0 and testing their functionalities.

4.2 Physical Dimensions

Table 2: Physical Dimensions

Item	Value
Length	100 mm
Width	70 mm
Height	25 mm

4.3 Interface Details

Connectors Position

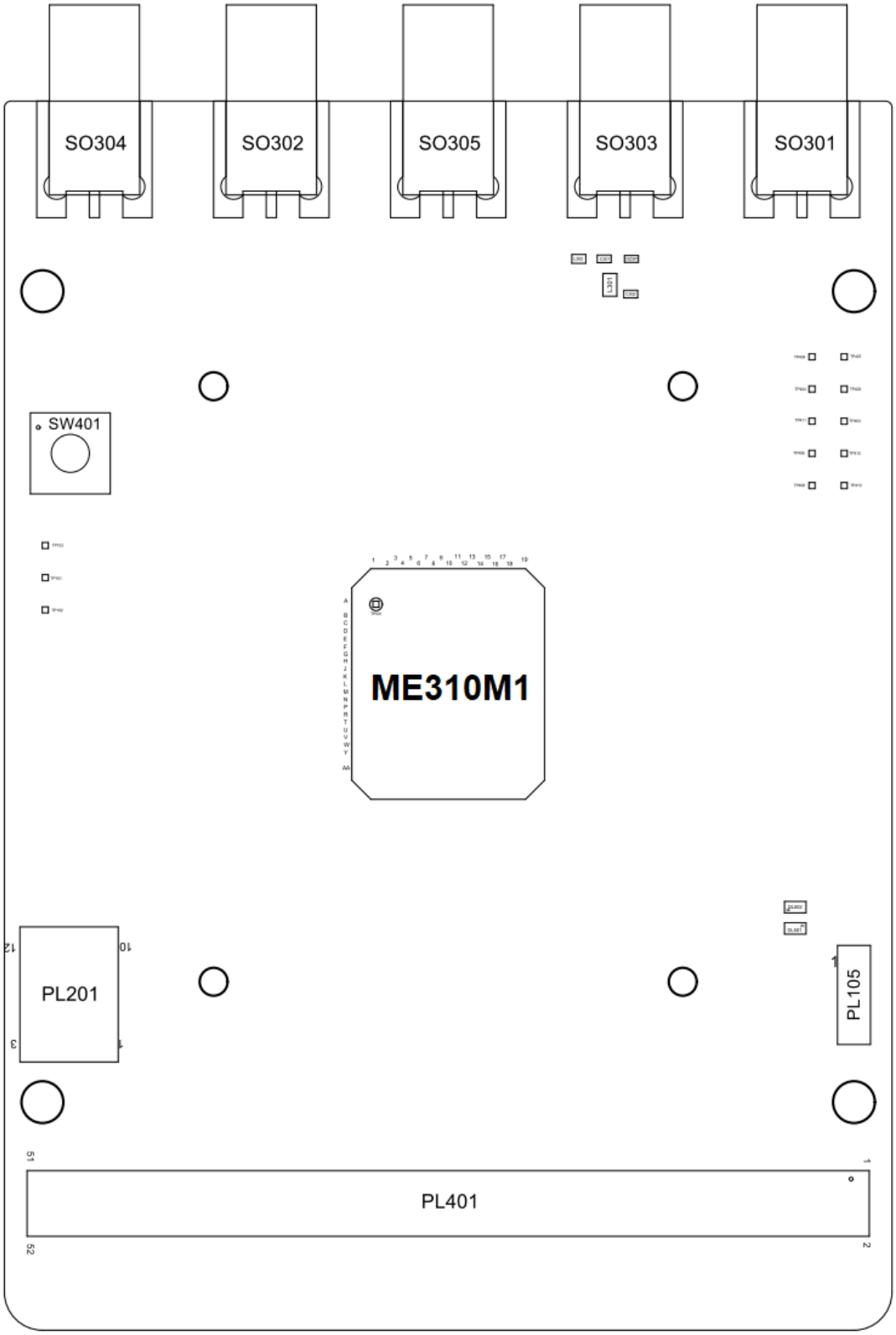


Figure 1; Connectors Position TOP SIDE

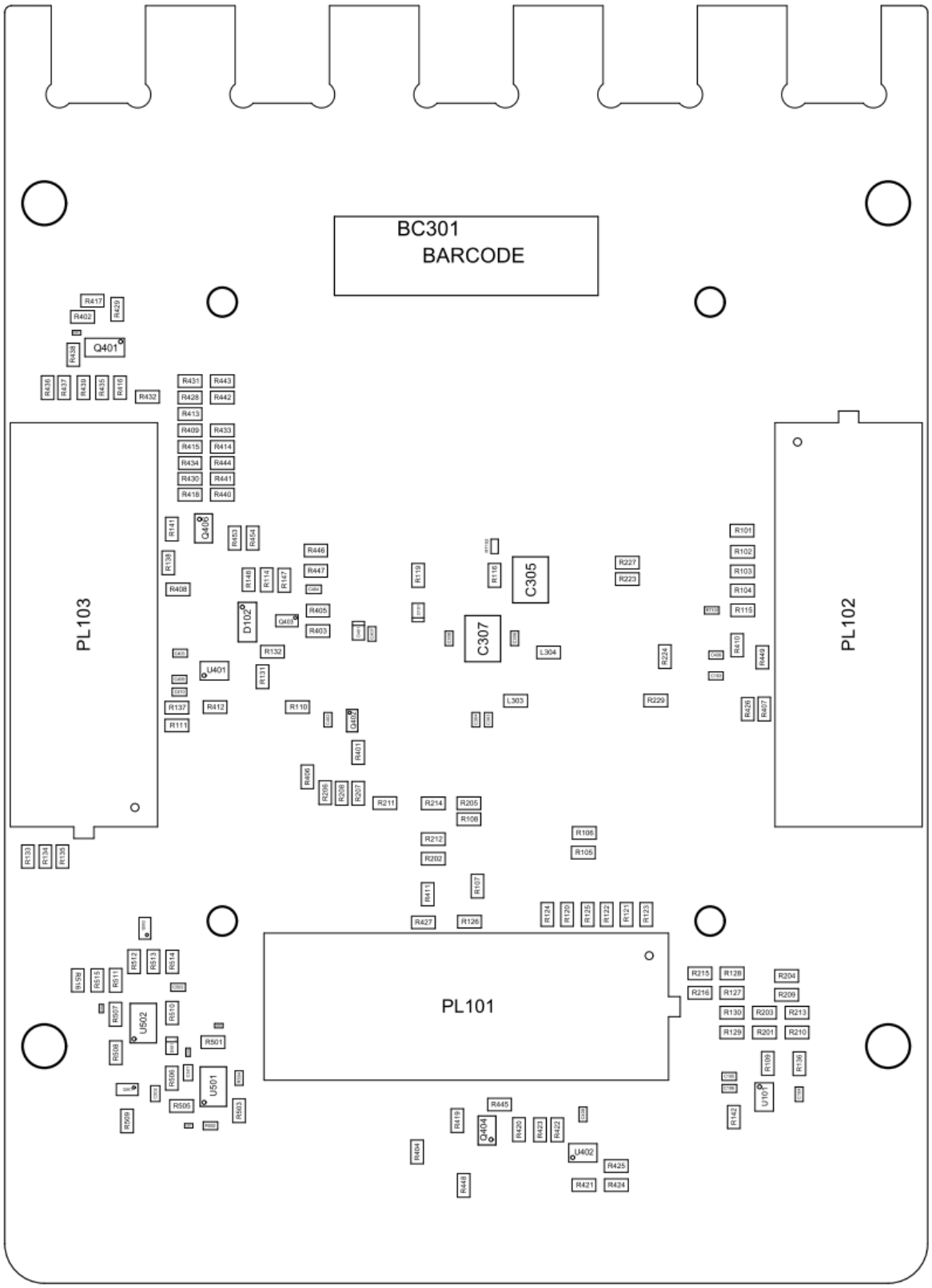


Figure 2; Connectors Position BOTTOM SIDE

Jumpers Setting

The following picture shows the jumpers placement and their default settings.

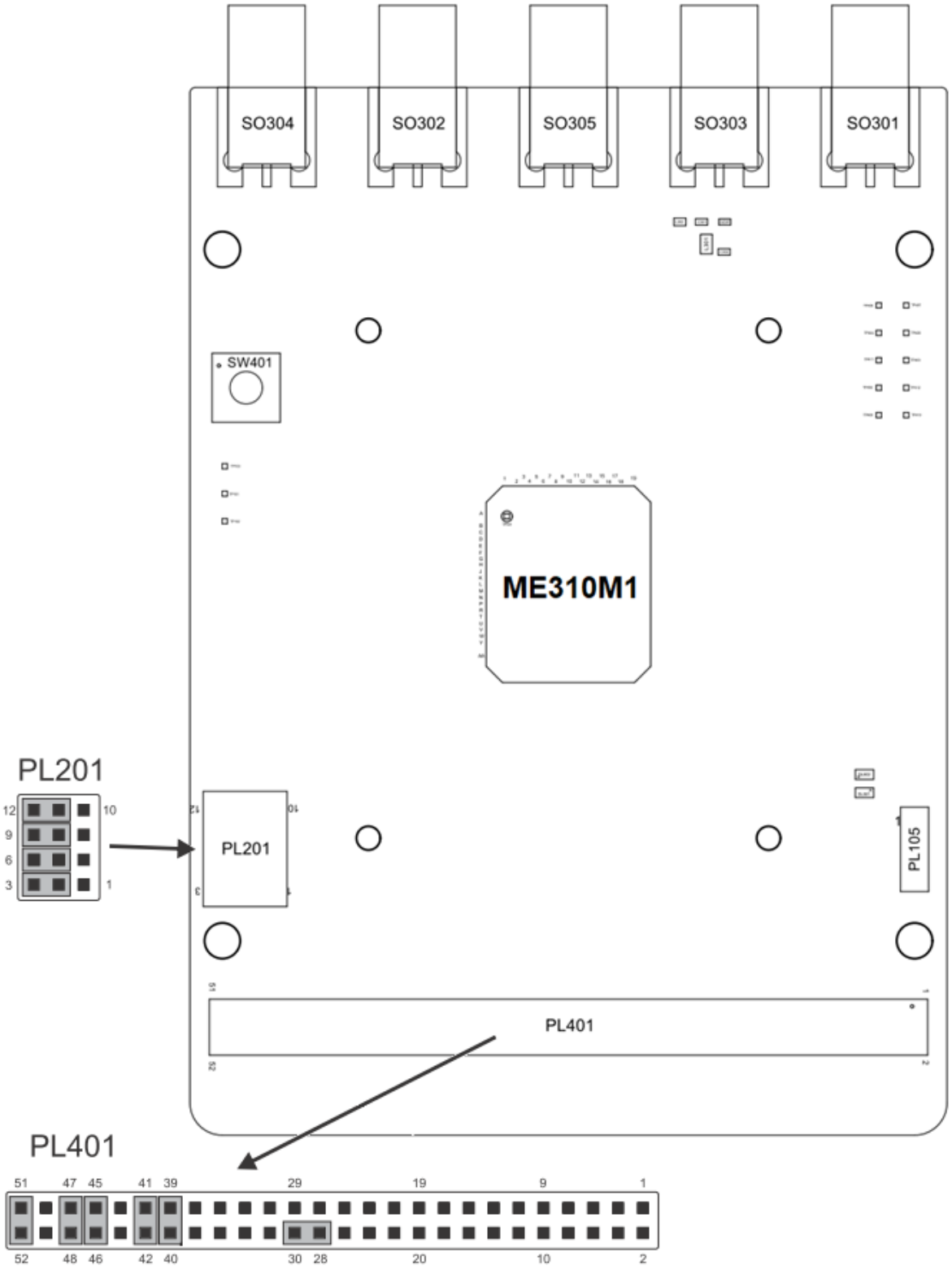


Figure 3: Jumper placement

5 PL101, PL102, PL103 – EVB 2.0 Connection

The connections between the Interface and the EVB 2.0 is done through three 6x20 pin connectors present on the bottom (PL101, PL102 and PL103).

The connector is a Samtec SEAM Series - .050" (1.27 mm) High Speed/High Density Open Pin Field with p/n is SEAM-20-09.0-L-06-2-A-K-TR

Theirs pin functions are listed in the following tables:

Table 3: PL101 Pin Functions

PL101											
1	GND	2	GND	3	NC	4	NC	5	GND	6	NC
7	NC	8	GND	9	Reserved	10	GPIO_06	11	NC	12	NC
13	NC	14	GND	15	GPIO_05	16	Reserved	17	NC	18	GND
19	GND	20	GND	21	VAUX/PWRMON2	22	VAUX/PWRMON2	23	GND	24	NC
25	NC	26	GND	27	NC	28	NC	29	NC	30	NC
31	NC	32	GND	33	NC	34	Reserved	35	NC	36	GND
37	GND	38	NC	39	NC	40	GPIO_04	41	GND	42	NC
43	Reserved	44	GPIO_02	45	GPIO_03	46	Reserved	47	NC	48	NC
49	VAUX/PWRMON1	50	VAUX/PWRMON1	51	NC	52	Reserved	53	NC	54	NC
55	NC	56	NC	57	GPIO_01	58	NC	59	NC	60	NC
61	NC	62	NC	63	NC	64	NC	65	NC	66	NC
67	Reserved	68	Reserved	69	ATC4	70	ATC1	71	NC	72	NC
73	Reserved	74	ATC3	75	Reserved	76	ATC2	77	NC	78	NC
79	GND	80	GND	81	Reserved	82	Reserved	83	NC	84	NC
85	NC	86	NC	87	NC	88	NC	89	C104/RXD1	90	NC
91	NC	92	NC	93	NC	94	NC	95	C103/TXD1	96	NC
97	NC	98	NC	99	NC	100	Reserved	101	NC	102	NC
103	Reserved	104	Reserved	105	Reserved	106	C105/RTS0	107	NC	108	NC
109	C104/RXD0	110	Reserved	111	C103/TXD0	112	C106/CTS0	113	Reserved	114	NC
115	NC	116	NC	117	NC	118	NC	119	NC	120	NC

Table 4: PL102 Pin Functions

PL102											
1	GPS_LNA_BIAS	2	GND	3	GPS_LNA_EN	4	NC	5	GND	6	NC
7	GND	8	GND	9	GND	10	GND	11	GND	12	NC
13	NC	14	NC	15	GND	16	NC	17	NC	18	NC
19	GND	20	GND	21	GND	22	GND	23	GND	24	GND
25	NC	26	NC	27	GND	28	NC	29	NC	30	GND
31	NC	32	NC	33	NC	34	NC	35	NC	36	NC

PL102											
37	GND	38	GND	39	NC	40	NC	41	GND	42	GND
43	NC	44	GND	45	GND	46	GND	47	GND	48	GND
49	NC	50	GND	51	GND	52	Reserved	53	Reserved	54	ADC_IN1
55	NC	56	NC	57	NC	58	NC	59	NC	60	NC
61	Reserved	62	Reserved	63	Reserved	64	Reserved	65	Reserved	66	GND
67	GND	68	GND	69	GND	70	GND	71	GND	72	NC
73	GND	74	GND	75	GND	76	GND	77	SIMVCC1	78	SIMVCC1
79	Reserved	80	NC	81	SIMCLK1	82	SIMIN1	83	SIMIO1	84	SIMRST1
85	NC	86	Reserved	87	NC	88	NC	89	NC	90	NC
91	Reserved	92	Reserved	93	NC	94	NC	95	NC	96	NC
97	GND	98	GND	99	NC	100	NC	101	NC	102	NC
103	Reserved	104	GND	105	NC	106	NC	107	NC	108	NC
109	Reserved	110	GND	111	NC	112	NC	113	NC	114	NC
115	GND	116	GND	117	NC	118	NC	119	NC	120	NC

Table 5: PL103 Pin Functions

PL103											
1	VBATT	2	VBATT	3	VBATT	4	VBATT_PA	5	VBATT_PA	6	VBATT_PA
7	VBATT	8	VBATT	9	VBATT	10	VBATT_PA	11	VBATT_PA	12	VBATT_PA
13	VBATT	14	VBATT	15	VBATT	16	VBATT_PA	17	VBATT_PA	18	VBATT_PA
19	NC	20	NC	21	NC	22	VBATT_PA	23	VBATT_PA	24	VBATT_PA
25	NC	26	NC	27	NC	28	NC	29	NC	30	NC
31	NC	32	NC	33	NC	34	NC	35	NC	36	NC
37	NC	38	NC	39	NC	40	NC	41	NC	42	NC
43	NC	44	NC	45	NC	46	NC	47	NC	48	NC
49	NC	50	NC	51	NC	52	NC	53	NC	54	NC
55	NC	56	NC	57	UART3_TXD	58	UART3_RXD	59	UART3_RTS	60	UART3_CTS
61	NC	62	NC	63	NC	64	NC	65	NC	66	NC
67	NC	68	NC	69	NC	70	NC	71	NC	72	NC
73	NC	74	NC	75	NC	76	NC	77	NC	78	NC
79	GND	80	GND	81	GND	82	GND	83	GND	84	GND
85	GND	86	GND	87	GND	88	GND	89	GND	90	GND
91	WAKEUP_B2B	92	ON_OFF	93	STAT_LED	94	NC	95	NC	96	RESET*_EVB
97	GND	98	GND	99	GND	100	GND	101		102	NC
103	1PPS	104	NC	105	NC	106	GND	107		108	NC
109	GND	110	GND	111	GND	112	GND	113	Reserved	114	Reserved
115	Reserved	116	Reserved	117	Reserved	118	Reserved	119	Reserved	120	Reserved

6 Antenna Connectors

6.1 SO304 – MAIN Antenna Connector

The MAIN Antenna is available on SO304 and it is a female SMA connector.

A compatible antenna (Refer to the product's HW Design guide) must be connected to SO304.

6.2 SO303 – GNSS Antenna Connector

The GNSS Antenna is available on SO303 and it is a female SMA connector.

A GNSS compatible antenna (Refer to the product's HW Design guide) has to be used.

6.3 WAKEUP push button

There are two dedicated wakeup signals for ME310M1 product, WAKE0 on pad P18 of the module and WAKE1 on pad T2 of the module.

These wakeup signals are active HIGH.

Asserting HIGH the WAKE1 on pad T2 is very simple, all you have to do is to push the button SW401 on the ME310M1 interface TLB.

Asserting HIGH the WAKE0 on pad P18 is a bit more complex: before you have to connect with a wired jumper pin 6 PL406 with pin 8 PL408 on the EVB 2.0, then all you have to do is to push the "spare" button SW603 on EVB 2.0.

7 SIM selector Connector

7.1 PL201

The connector carries the following signals:

Table 6: PL201 connector signals

Pin	Signal	Function
1	M2M_SIMRST	SIM reset: To M2M SIM inside the module (not for all module configurations)
2	SIMRST	SIM reset: From microcontroller inside the module
3	SIMRST1	SIM reset: To EVB 2.0 SIM holder (External SIM)
4	M2M_SIMIO	SIM data: To M2M SIM inside the module (not for all module configurations)
5	SIMIO	SIM data: From microcontroller inside the module
6	SIMIO1	SIM data: To EVB 2.0 SIM holder (External SIM)
7	M2M_SIMCLK	SIM clock: To M2M SIM inside the module (not for all module configurations)
8	SIMCLK	SIM clock: From microcontroller inside the module
9	SIMCLK1	SIM clock: To EVB 2.0 SIM holder (External SIM)
10	M2M_VSIM	SIM supply: To M2M SIM inside the module(not for all module configurations)
11	SIMVCC	SIM supply: From microcontroller inside the module
12	SIMVCC1	SIM supply: To EVB 2.0 SIM holder (External SIM)

PL201 default jumper setting is for External SIM.

8 Expansion Connectors

8.1 PL401

The connector carries the following signals:

Table 7: PL401 connector signals

Pin	Signal	Function
1	VBATT_AUX	Interface Power supply
2	Reserved	Reserved
3	NC	
4	GPIO_06	General Purpose IO #6
5	GPIO_05	General Purpose IO #5
6	ATC4	Antenna Tuner Control
7	GPIO_04	General Purpose IO #4
8	GPIO_03	General Purpose IO #3
9	GPIO_02	General Purpose IO #2
10	GPIO_01	General Purpose IO #1
11	WAKEUP_T2	Wake-Up signal from DHx status
12	GND	Ground
13	1V8	1.8V supply
14	I2C_SCL_B2B	I2C clock
15	1PPS	PPS output signal from GNSS receiver
16	C108/DTR	Reserved for HW flow control with GPIO
17	Reserved	Reserved
18	PWRMON	PWRMON from module
19	Reserved	Reserved
20	DAC_OUT	Digital To Analog Converter
21	C109/DCD	Reserved for HW flow control with GPIO
22	GND	Ground
23	C125/RING	Reserved for HW flow control with GPIO
24	Reserved	Reserved
25	C107/DSR	Reserved for HW flow control with GPIO
26	ATC4	Antenna Tuner Control
27	Reserved	Reserved
28	GNSS_LNA_EN	GNSS external LNA enable
29	VBATT_AUX	VBATT input to supply the Interface circuitry
30	GNSS_LNA_EN_EVB	GNSS LNA enable line from EVB 2.0
31	C104/RXD1	Serial data output (RXD) to DTE (Secondary UART)
32	C103/TXD1	Serial data input (TXD) from DTE (Secondary UART)
33	TX_TRACE_EVB	To EVB 2.0

Pin	Signal	Function
34	RX_TRACE_EVB	To EVB 2.0
35	TX_AUX	Auxiliary UART (TX Data to DTE)
36	RX_AUX	Auxiliary UART (RX Data from DTE)
37	C103/TXD1	Serial data input (TXD) from DTE (Secondary UART)
38	C104/RXD1	Serial data output (RXD) to DTE (Secondary UART)
39	GPIO_04	General purpose IO #4
40	SIMIN1	SIM detect signal from EVB 2.0 SIM holder
41	C104/RXD	To EVB 2.0
42	C104/RXD0	Serial data output (RXD) to DTE (Main UART)
43	C104/RXD1	Serial data output (RXD) to DTE (Secondary UART)
44	C106/CTS1	Output for Clear to send signal (CTS) to DTE (Secondary UART)
45	C106/CTS0	Output for Clear to send signal (CTS) to DTE (Main UART)
46	C106/CTS	To EVB 2.0
47	C103/TXD	To EVB 2.0
48	C103/TXD0	Serial data input (TXD) from DTE (Main UART)
49	C103/TXD1	Serial data input (TXD) from DTE (Secondary UART)
50	C105/RTS1	Input for Request to send signal (RTS) from DTE (Secondary UART)
51	C105/RTS0	Input for Request to send signal (RTS) from DTE (Main UART)
52	C105/RTS	To EVB 2.0

There are Jumpers on this PL401 connector that permit to select the following:

- To connect the Main UART (UART0) to EVB 2.0 level translators (41-42, 45-46, 47-48, 51-52). This is the default jumper settings.
- To connect the Secondary UART (UART1) to the EVB 2.0 level translators (41-43, 44-46, 47-49, 50-52). Connected as default to EVB 2.0 UART3 with R210, R212, R213 and R214.
- To connect the Auxiliary UART to the EVB 2.0 AUX UART level translators (33-35 and 34-36)

In case is needed to connect an external application to the Main UART, Secondary UART, Auxiliary UART or simply to isolate them from the rest of the circuitry it is only needed to remove the jumpers.

Please refer to ANNEX 1 ME310M1 Interface TLB Schematic **for interface Electric Diagrams and** ANNEX 2 ME310M1 Interface TLB Components Layout **for components layout.**

9 ANNEX 1 ME310M1 Interface TLB Schematic

Restricted document. No part of this document can be reproduced or copied in any format, in part or totally, nor its contents revealed in any manner to others without the express written permission of Telit Cinterion. All rights reserved.

VAUX/PWRMON

R131 0 R 0603

RES_N4 — R132 0 R 0603 (DNI)

RES_J16 — R147 0 R 0603 (DNI)

D102 BAS70-07,215

R114 0 R 0603

R148 100 K 5% 0603 (DNI)

GND

L

PL102 SEAM-20-09.0-L-06-2-A-K-TR

GPS_LNA_BIAS

GNSS_LNA_EN_EVB

DVI_TX — R101 0 R 0603 (DNI)

DVI_CLK — R102 0 R 0603 (DNI)

DVI_RX — R103 0 R 0603 (DNI)

DVI_WAO — R104 0 R 0603 (DNI)

TP102

ADC_IN1

DAC_OUT

DVI_WAO_1V8

DVI: DVI_RX_1V8, DVI_TX_1V8, DVI_CLK_1V8

SIMVCC1

SIMIN1

SIMIO1

SIMRST1

C103 2.2 uF 0402 10 V X5R

SIMCLK1

USB_VBUS

RES_U19

RES_V18

GND

C

PL101 SEAM-20-09.0-L-06-2-A-K-TR

TP101

TP103

I2C_SDA_B2B — R106 0 R 0603

I2C_SCL_B2B — R105 0 R 0603

GPIO_05 — R128 0 R 0603

GPIO_06 — R127 0 R 0603

FORCED_BOOT

SPI_MOSI

SPI_MISO

SPI_CLK

SPI_CS

GPIO_02 — R107 0 R 0603

GPIO_03 — R130 0 R 0603

GPIO_04 — R129 0 R 0603

C-49-50

GPIO_01 — R108 0 R 0603

VMMC

SD_CD/ATC4 — R126 0 R 0603

M2M_VSIM — R120 0 R 0603 (DNI)

ATC3 — R125 0 R 0603

M2M_SIMIO — R122 0 R 0603 (DNI)

R121 0 R 0603 — ATC1

R124 0 R 0603 — ATC2

R123 0 R 0603 (DNI) — M2M_SIMCLK

TX_TRACE_1V8 / RTS_AUX

RX_TRACE_1V8 / CTS_AUX

C107/DSR

C125/RING

C104/RXD0_1V8

C109/DCD

C103/TXD0_1V8

C105/RTS0_1V8

C106/CTS0_1V8

C108/DTR

GND

R

PL103 SEAM-20-09.0-L-06-2-A-K-TR

VBATT_EVB

VBATT_PA_EVB

VBATT_AUX_EVB

EVB_LDO_ADJ

EVB_DCDC_ADJ

EVB_DCDC_OUTPUT

3V8_EVB

Module power supply selection:
- Vbatt = 1.8V, with R133 = 6.2K 1%
- Vbatt = 3.3V, with R133 = 2.2K 1%
- Vbatt = 3.8V, with R133 = 1.8K 1%

EVB_GND

R133 1.80 K 1% 0603

R134 2.7 K 1% 0603 (DNI)

R135 10 K 1% 0603

Vddio selection:
- R135 mount 2.8V
- R135 no mount 1.8V (default)

PIN 79: leave this pin N.C. (it is used by the new EVB to generate the right supply voltage for the oldest TLB)

RESET*_EVB — R138 0 R 0603 — R-96

WAKEUP_B2B — R141 0 R 0603

ON_OFF*

STAT_LED

C105/RTS

D101 BAS70-02W H6327 (DNI)

R119 0 R 0603

1PPS

UART3_RXD

UART3_RTS

UART3_CTS

UART3_TXD

JTAG_DETECT_CONN

HW_KEY_SENSE

R115 0 R 0603 (DNI)

R116 0 R 0603

RT101 10 K 1% 0402

RT102 10 K 1% 0402

JTAG_TRIGOUT_CONN

JTAG_TRIGIN_CONN

JTAG_SUPPLY_CONN

JTAG_PS_HOLD_CONN

JTAG_TDI_CONN

JTAG_TMS_CONN

JTAG_TDO_CONN

JTAG_TRST_CONN

JTAG_TCK_CONN

JTAG_RTCK_CONN

JTAG_RESET_CONN

GND

B2B CONNECTORS

VAUX

R110 0 R 0603

VAUX/PWRMON

C-49-50

R109 0 R 0603

R136 0 R 0603 (DNI)

PL105 4711955103400 (DNI)

C104 2.2 uF 10 V 0402 X5R (DNI)

LP5951MGX-1.8/NOPB U101 (DNI)

R142 100 K 5% 0603

C105 33 pF 50 V 0402 C0G

C106 1 uF 10 V 0402 X5R

VBATT_AUX

VBATT_AUX_EVB

R111 0 R 0603

R137 0 R 0603 (DNI)

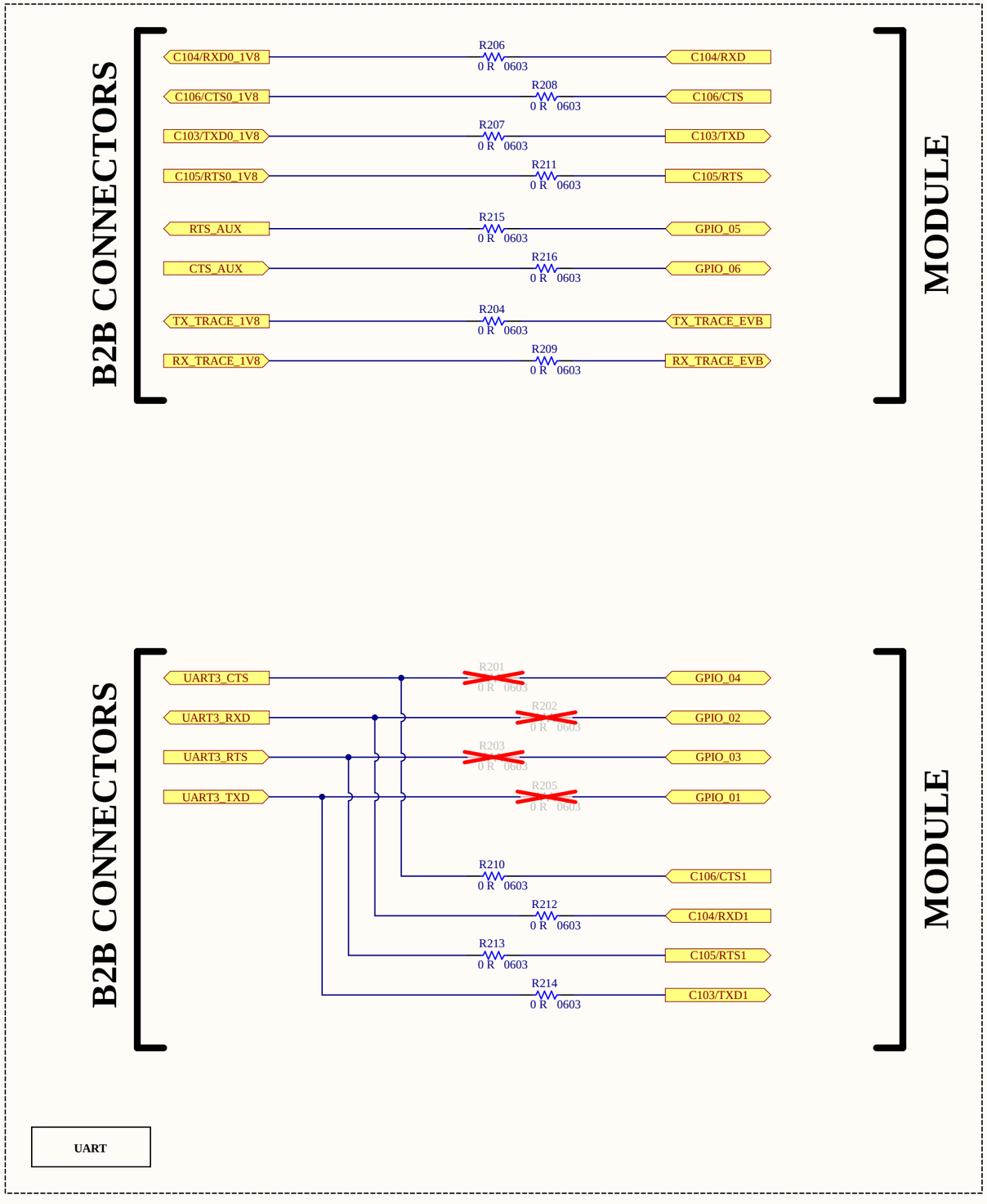
3V8_EVB

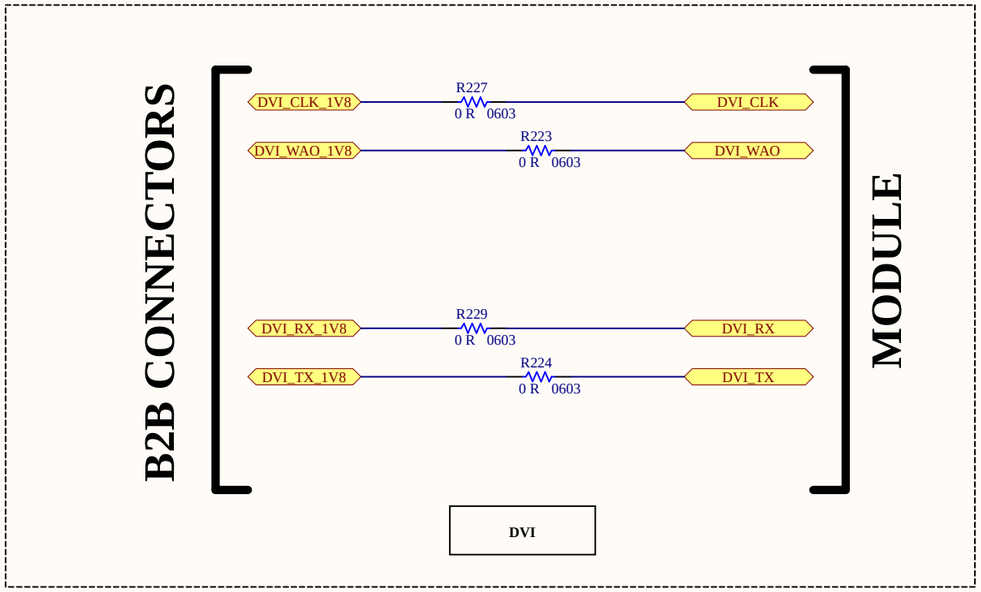
GND

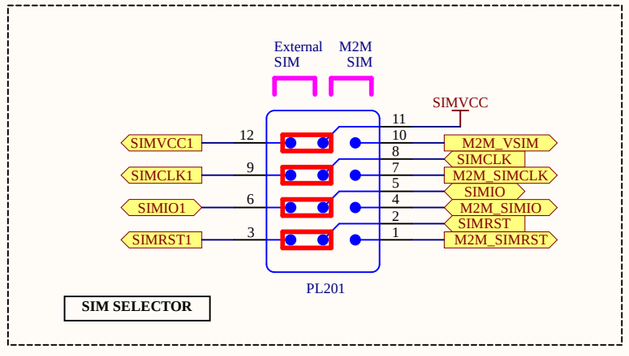
DATE: 14/03/2024	DESCRIPTION: ME310M1-W1/W2 INTERFACE TLB
FILE NAME: cs2137a-D	ANNOTATION: Refer to 1VV0301897 Rev.1 HUG
	FORM: A3
	SHEET N.: 1
	OF SHEETS: 5

Telit Cinterion

Restricted document. No part of this document can be reproduced or copied in any format, in part or totally, nor its contents revealed in any manner to others without the express written permission of Telit Cinterion.
All rights reserved.

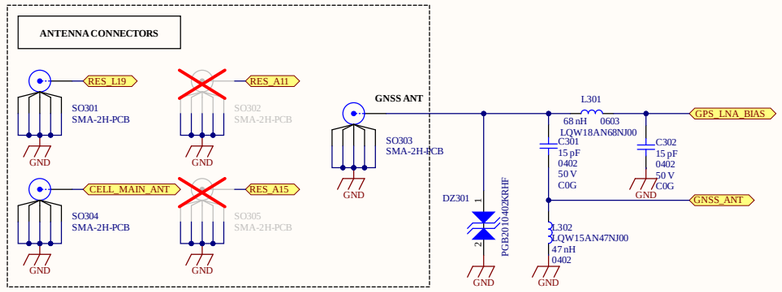


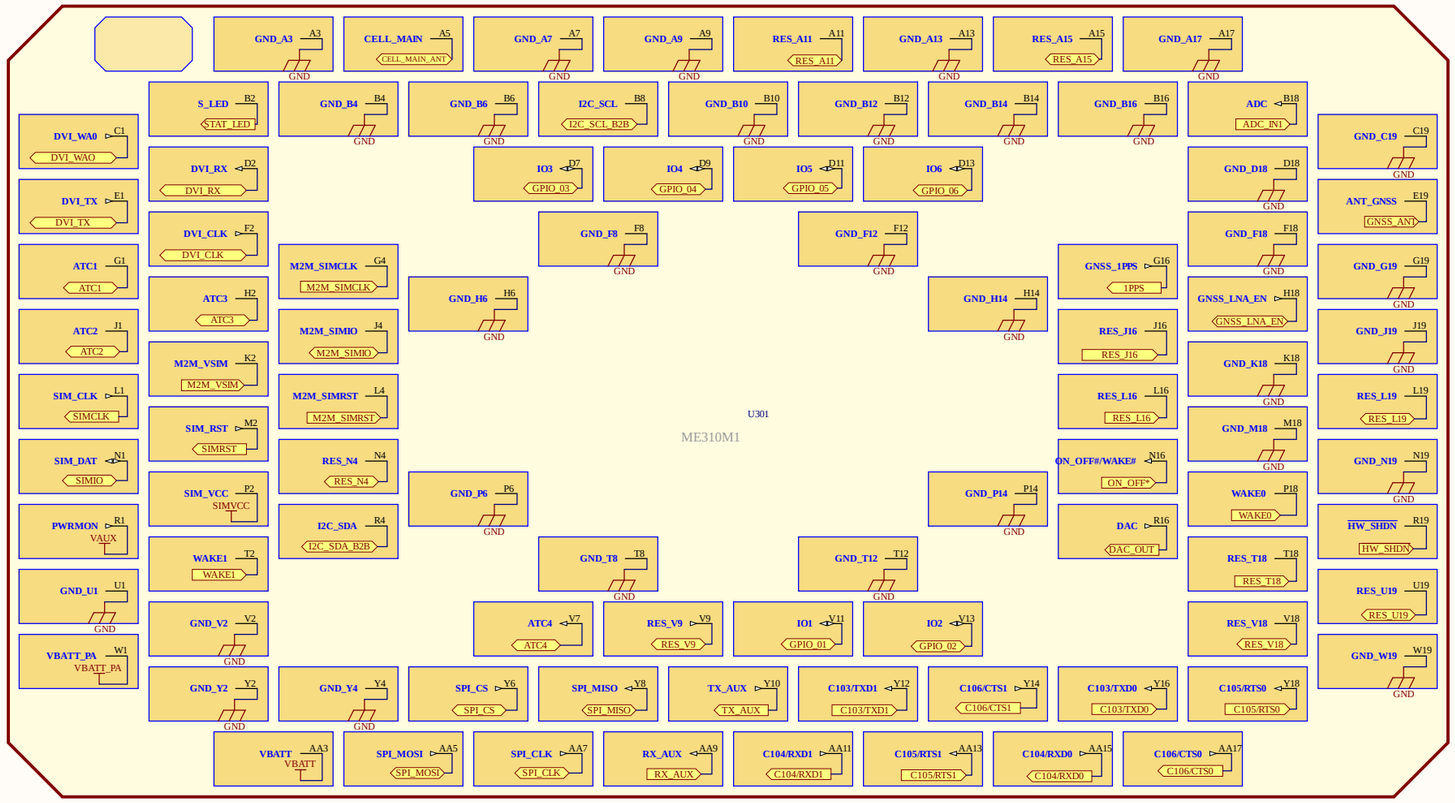


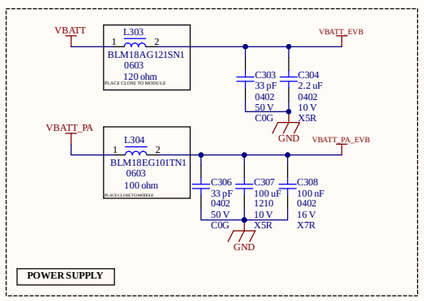


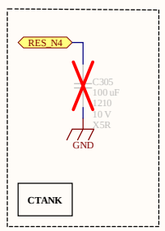
DATE: 14/03/2024	Telit Cinterion	DESCRIPTION: ME310M1-W1/W2 INTERFACE TLB	
FILE NAME: cs2137a-D		ANNOTATION: Refer to 1VV0301897 Rev.1 HUG	FORM: A3
		SHEET N.: 2	OF SHEETS: 5

Restricted document. No part of this document can be reproduced or copied in any format, in part or totally, nor its contents revealed in any manner to others without the express written permission of Telit Cinterion.
All rights reserved.









BC301
BARCODE

DATE: 14/03/2024		DESCRIPTION: ME310M1-W1/W2 INTERFACE TLB	
FILE NAME: cs2137a-D		ANNOTATION: Refer to 1VV0301897 Rev.1 HUG	FORM: A2
		SHEET N.: 3	OF SHEETS: 5

Restricted document. No part of this document can be reproduced or copied in any format, in part or totally, nor its contents revealed in any manner to others without the express written permission of Telit Cinterion. All rights reserved.

RESET

RESET*_CONN
R401 0 R 0603
KEEP THIS PATH SHORT
HW_SHDN
Q402 MMBT2222AT-TP
C407 10 pF 0402 50 V C0G
C402 33 pF 0402 50 V C0G
D401 BAS70-02W H6327
JTAG_RESET*
Close to pad R19 U301
VBATT_AUX
R403 47 K 5% 0603
R405 12 K 5% 0603
Q403 DTC144EET1G
R408 0 R 0603
RESET*_EVB
C404 470 nF 0402_C_PLUS1 10 V X5R
GND

WAKEUP_pad_P18

USB_VBUS
R407 0 R 0603
(T18)
RES_T18
R426 100 K 1% 0603
Use RESET or SPARE_PB button on the EVB2.0
WAKEUP_B2B
Q406
RN2307(TE85L,F)
1V8
R453 0 R 0603
WAKE0
R454 0 R 0603

WAKEUP_pad_T2/FORCED_USB_BOOT

WAKE1
R411 18 K 5% 0603
RES_N4
R427 0 R 0603
1V8
R404 0 R 0603
WAKEUP_pad_T2
SW401 MJTPSJW69N
VAUX
R406 0 R 0603
Q404
RN2307(TE85L,F)
R419 33 R 5% 0603
FORCED_BOOT
R420 0 R 0603
FORCED_USB_BOOT button on the EVB2.0
R445 0 R 0603
C109/DCD
C125/RING
C107/DSR
HW flow control with GPIO

GPIO CONNECTOR

VBATT_AUX
PL401
R446 1 K 5% 0603
R447 1 K 5% 0603
RES_J16
RESET*_CONN
GPIO_06
SD card detect
GPIO_05
SD card detect/ATC4
GPIO_04
GPIO_03
GPIO_02
GPIO_01
SD_CD/ATC4
R448 0 R 0603
ATC4
11-12: to GND
11-13: pull-up
I2C_SCL_B2B
1PPS
C108/DTR
VAUX/PWRMON
SD supply en.
VMMC
SD supply en.
RES_L16
DAC_OUT
RES_N4
ATC4
RES_V9
GNSS_LNA_EN
GNSS_LNA_EN_EVB
GNSS_LNA
2B-30: GNSS_LNA_EN
29-30: ALWAYS ON
AUX UART and UART1 connections:
A) AUX UART <-> UART1
B) UART1 to EVB
C) AUX UART to EVB
C104/RXD1
C103/TXD1
TX_TRACE_EVB
TX_AUX
Recovery
RX_AUX
RX_TRACE_EVB
SIM DETECT
GPIO_04
C104/RXD
C104/RXD0
C106/CTS1
C106/CTS
C103/TXD0
C105/RTS1
C105/RTS
UART0 with RTS0 and CTS0
UART1 with RTS1 and CTS1
connections:
D) UART0 to EVB
E) UART1 to EVB
WARNING!
E) configuration not allowed if B) or A) configurations are used.
WARNING!
(ME310G1 only)
E) configuration not allowed if UART1 connected to UART3 EVB (mounted jumpers PL1003 for CS2148 and jumpers PL903 for CS2115).
C106/CTS0
C103/TXD
C103/TXD1
C105/RTS0
TSM-126-01-S-DV
RES_N4
R410 470 K 5% 0603
SIMIN1
VAUX
R449 470 K 5% 0603
C406 10 nF 0402 25 V X7R

JTAG

1V8
R409 0 R 0603
VAUX/PWRMON
R433 0 R 0603
R413 10 K 5% 0603
R414 10 K 5% 0603
R415 10 K 5% 0603
R416 5.1 K 5% 0603
TP406
R402 0 R 0603
C401 0201 10 V 100 nF X5R
GND
TP412
JTAG_PS_HOLD
Q401 SI2333CDS-T1-GE3
R417 5% 0603 91 K
R429 0 R 0603
TP407
TP403
TP404
TP409
R418 0 R 0603
R428 0 R 0603
R430 0 R 0603
R431 0 R 0603
R432 0 R 0603
R440 0 R 0603
R441 0 R 0603
R442 0 R 0603
R443 0 R 0603
WAKE1
GPIO_02
GPIO_04
GPIO_03
GPIO_01
R444 0 R 0603
TP405
R434 33 R 5% 0603
TP411
R435 0 R 0603
JTAG_RESET*
TP410
R436 0 R 0603
TP408
R437 0 R 0603
R438 220 K 5% 0603
JTAG_PS_HOLD_CONN
R439 0 R 0603
JTAG_PS_HOLD

JTAG_SUPPLY_CONN	NC
JTAG_TRST_CONN	GND
JTAG_TDI_CONN	GND
JTAG_TMS_CONN	JTAG_DETECT_CONN
JTAG_TCK_CONN	GND
JTAG_RTCK_CONN	GND
JTAG_TDO_CONN	GND
JTAG_RESET_CONN	GND
JTAG_TRIGIN_CONN	GND
JTAG_TRIGOUT_CONN	GND

JTAG connector schema
(JTAG EVB pins on the "R" B2B Connector)

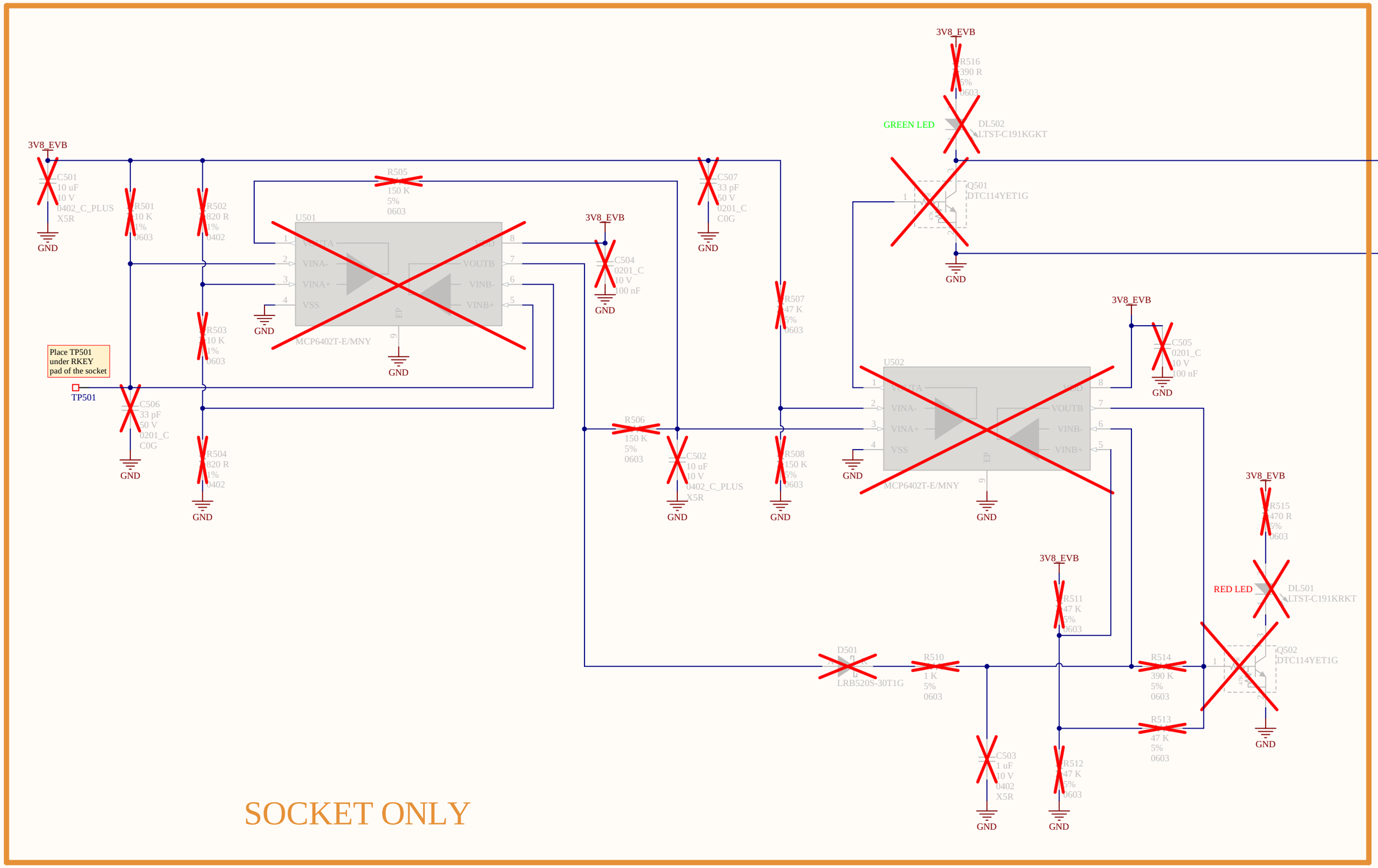
1V8
U401 LP5951MGX-1.8/NOPB
C403 2.2 uF 0402 10 V X5R
VBATT_AUX
R412 0 R 0603
C409 33 pF 0402 50 V C0G
C410 1 uF 0402 10 V X5R
GND

RECOVERY BUTTON

VBATT_AUX
R422 10 K 5% 0603
R423 0 R 0603
FORCED_BOOT
Use FORCED_USB_BOOT button on the EVB2.0
C408 100 nF 16 V 0402 X7R
U402
R424 0 R 0603
RX_TRACE_EVB
TX_TRACE_EVB
R425 0 R 0603
RX_AUX
TX_AUX

DATE: 14/03/2024		DESCRIPTION: ME310M1-W1/W2 INTERFACE TLB	
FILE NAME: cs2137a-D		ANNOTATION: Refer to 1VV0301897 Rev.1 HUG	FORM: A3
		SHEET N.: 4	OF SHEETS: 5

Restricted document. No part of this document can be reproduced or copied in any format, in part or totally, nor its contents revealed in any manner to others without the express written permission of Telit Cinterion.
All rights reserved.

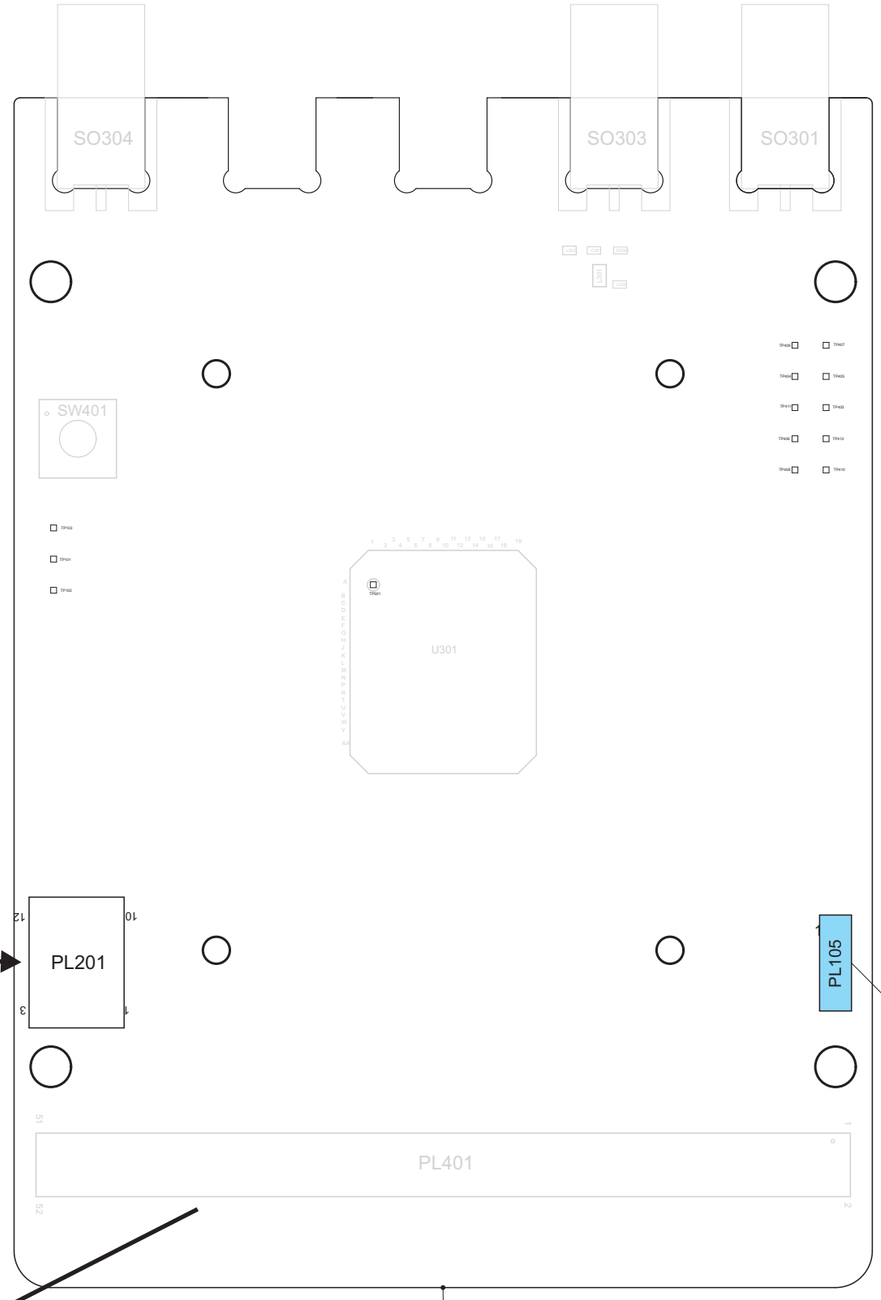


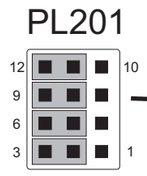
SOCKET ONLY

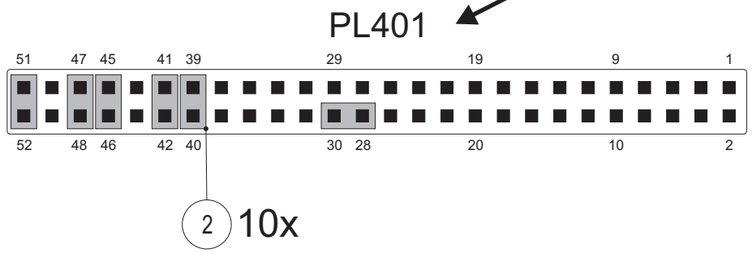
DATE: 14/03/2024	Telit Cinterion	DESCRIPTION: ME310M1-W1/W2 INTERFACE TLB
FILE NAME: cs2137a-D	ANNOTATION: Refer to 1VV0301897 Rev.1 HUG	FORM: A3
	SHEET N.: 5	OF SHEETS: 5

10 ANNEX 2 ME310M1 Interface TLB Components Layout

ALL RIGHTS RESERVED! REPRODUCTION AND DISCLOSURE FORBIDDEN







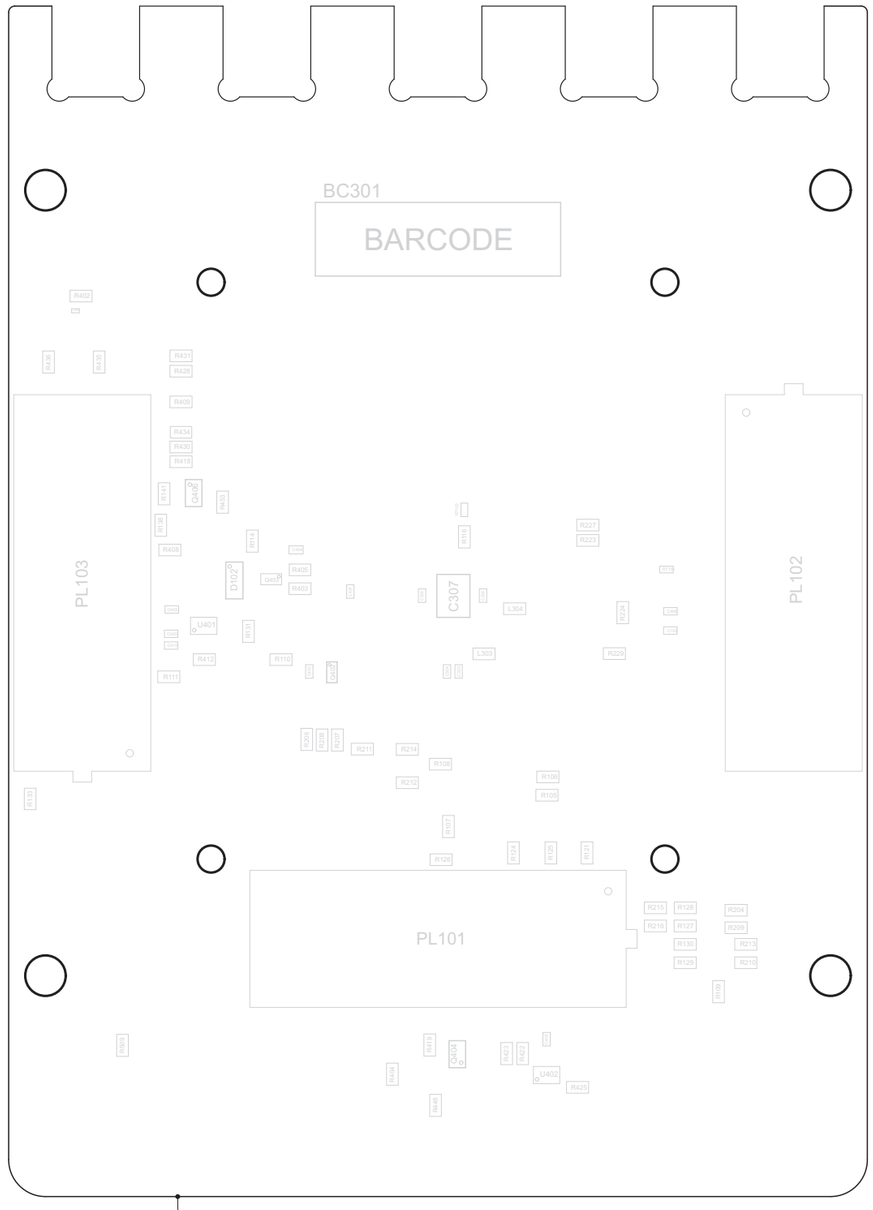
1

PL105

NOT MOUNTED
PTH COMPONENTS

MODIFY												
DATE	2024-03-26											
PATH		Telit Cinterion			DESCRIPTION							
FILE NAME					ME310M1-W1/W2 INTERFACE TLB CS2137a-D							
FILE GERBER												
SCALE 2:1		ANNOTATION									FORM	
Mod. 048 rev. 11/2023		Final Assembly - TOP SIDE									A3	
Drawn by		Project			SHEET N.		OF SHEETS		DRAWING CODE			
Verif. by					1		2					

ALL RIGHTS RESERVED! REPRODUCTION AND DISCLOSURE FORBIDDEN



1

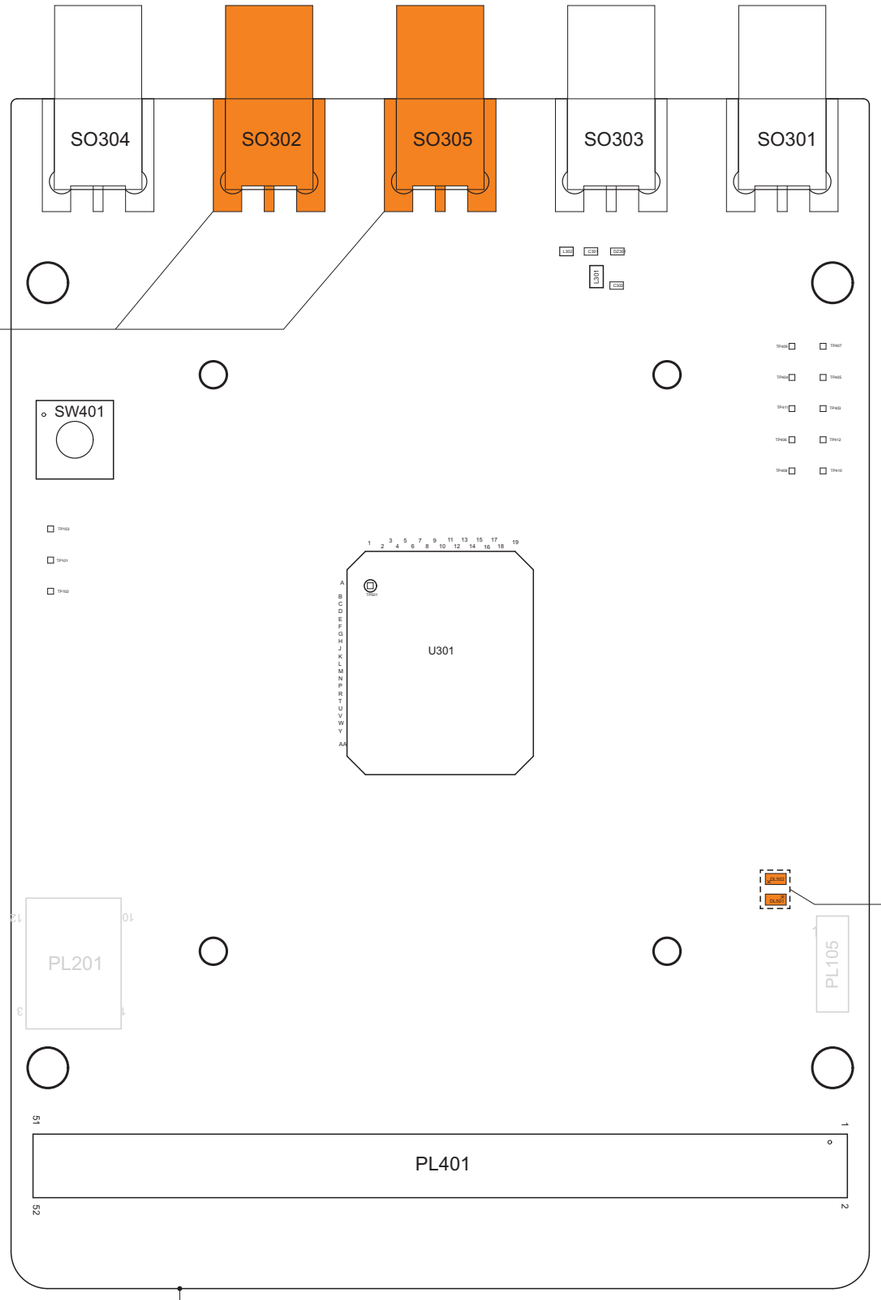
MODIFY												
DATE	2024-03-26											

PATH	Telit Cinterion	DESCRIPTION: ME310M1-W1/W2 INTERFACE TLB CS2137a-D
FILE NAME		
FILE GERBER		
SCALE 2:1	ANNOTATION: Final Assembly - BOTTOM SIDE	FORM: A3
Mod. 048 rev. 11/2023		

Drawn by	Project	SHEET N.	OF SHEETS	DRAWING CODE
Verif. by		2	2	

ALL RIGHTS RESERVED! REPRODUCTION AND DISCLOSURE FORBIDDEN

SO302 SO305



DL502 DL501

NOT MOUNTED SMD COMPONENTS

MODIFY												
DATE	2024-03-26											
PATH			Telit Cinterion		DESCRIPTION							
FILE NAME					ME310M1-W1/W2 INTERFACE TLB CS2137a-D							
FILE GERBER												
SCALE 2:1			ANNOTATION								FORM	
Mod. 048 rev. 11/2023			Primary Layer Layout								A3	
Drawn by			Project		SHEET N.		OF SHEETS		DRAWING CODE			
Verif. by					1		1					

ALL RIGHTS RESERVED! REPRODUCTION AND DISCLOSURE FORBIDDEN

R417 R429 R438 R437 R439
Q401 R416 R432 R413 R415
R443 R442 R433 R414 R444
R441 R440

R454 R148 R147 R446 R447
D401 D101 R119 R132 R137
R406 R401

R134 R135 R205 R202 R411
R427

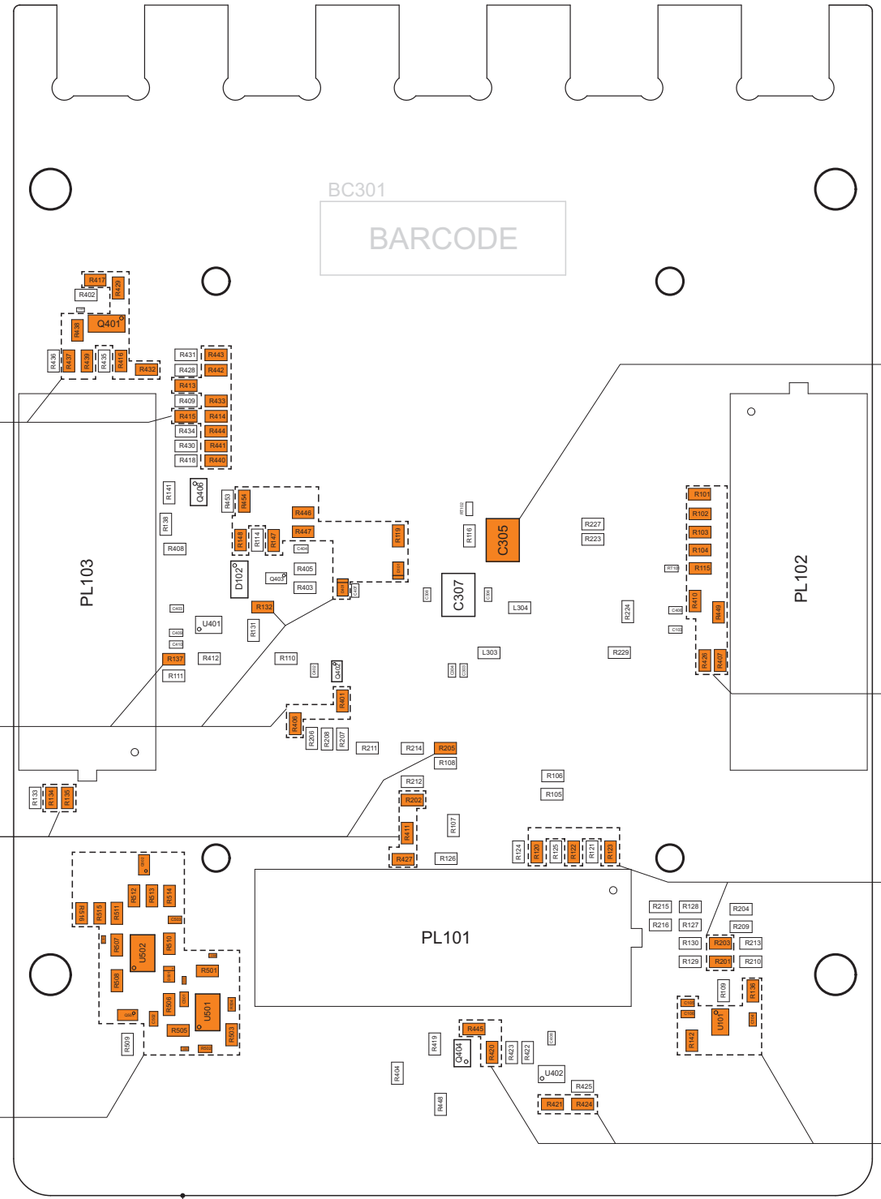
Q502 R512 R513 R514 R516
R515 R511 C503 C504 R507
U502 R510 R508 Q501 C502
R506 D501 C505 C501 C506
R501 U501 R504 R503 R502
R505 C507

C305

R101 R102 R103 R104 R115
R410 R449 R426 R407

R120 R122 R123 R203 R201

R445 R420 R421 R424 C105
C106 R142 U101 C104 R136



1

NOT MOUNTED SMD COMPONENTS

MODIFY												
DATE	2024-03-26											
PATH			Telit Cinterion		DESCRIPTION							
FILE NAME					ME310M1-W1/W2 INTERFACE TLB CS2137a-D							
FILE GERBER												
SCALE 2:1			ANNOTATION									FORM
Mod. 048 rev. 11/2023			Secondary Layer Layout									A3
Drawn by			Project			SHEET N.	OF SHEETS	DRAWING CODE				
Verif. by						1	1					

11 Acronyms and Abbreviations

Table 8: Acronyms and Abbreviations

Acronym	Definition
TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

12 Related Documents

Refer to https://dz.telit.com/ for current documentation and downloads.

Table 9: Related Documents

S.no	Book Code	Document Title
1	1VV0301774	Telit EVB 2.0 User Guide
2	1VV0301897	ME310M1 HW Design Guide
3	80756ST11189A	ME310M1 AT Commands Reference Guide

13 Document History

Table 10: Document History

Revision	Date	Changes
0	2024/04/04	First issue

From Mod.0818 Rev.12

© Telit Cinterion. All rights reserved.

Technical Documentation